ACADEMIC REGULATIONS FOR B.TECH PROGRAMME UNDER AUTONOMOUS STATUS

(W.E.F. THE ADMITTED BATCH OF 2020-21)

HONORS/ MINOR PROGRAMME FRAMEWORK:

i) A candidate shall be eligible to register for Honor or Minor degree along with regular B.Tech degree. A candidate shall earn 20 credits in addition to the 160 credits to get Honor / Minor degree along with regular B.Tech degree. A candidate shall be permitted to register either for Honors or for Minor and not for both simultaneously.

ii) A candidate shall be permitted to register for Honors / Minor program at the beginning of4th semester subject to a maximum of two additional courses per semester, provided that the student must have acquired a minimum of 8.00 CGPA up to the end of 2ndsemester without any backlogs. In case of the declaration of the 3rd semester results after the commencement of the 4th semester and if a candidate fails to score the required minimum of 8.00 CGPA, his/her registration for Honors / Minor Programme stands cancelled and he/she shall continue with the regular Programme.

iii) In case a student fails to meet the CGPA requirement for Degree with Honors / Minor at any point after registration, he/she will be dropped from the list of students eligible for Degree with Honors / Minors and they will receive regular B.Tech degree only. However, such students will receive a separate grade sheet mentioning the additional courses completed by them.

iv) Honors / Minor must be completed simultaneously with a major degree program. A student cannot earn Honors/ Minor after he/she has already earned bachelor's degree.

v) A Candidate iseligibletooptforHonorsProgrammeofferedbytheconcernedDepartment/Discipline and he/she will be awarded B.Tech. (Honors) in the concerned Discipline.

vi) Candidates who are desirous of pursuing their special interest areas in chosen discipline of Engineering may opt for additional courses in minor specialization groups(Specialized Tracks) offered by the concerned department and he/she will get Major degree of concerned Discipline with minor degree of Specialized Track.

vii) Candidates who are desirous of pursuing their special interest areas other than the chosen discipline of Engineering may opt for additional courses in minor specialization groups (General Tracks) offered by the department other than their parent department and he/she will get Major degree of concerned Discipline with minor degree in other department.

viii) CandidatescanalsooptforIndustryrelevanttracksofanybranchlikeDataMiningtrack,IOTtrack,Machinelearningtracketcorindustrytrackssuchas ArtificialIntelligence (AI), Machine Learning (ML), Data Science (DS), Robotics, Electric vehicles, VLSI etc. to obtain the Minor Degree and he/she will get Major degree of concerned discipline with minor degree in industry track.

ix)In the case of Honors, out of 20 additional Credits to be acquired, 16 credits shall be earned by undergoing specified courses listed as pools, with four courses, each carrying4 credits. The

remaining 4 credits must be acquired through two MOOCs courses, which shall be domain specific, each with 2 credits and with a minimum duration of 8 weeks as recommended by the Board of studies.If the MOOC course is a pass course without anygrades,the gradeto beassignedas decidedby the AcademicCouncil.

x)In the case of Minor, out of 20 additional Credits to be acquired, 16 credits shall beearnedbyundergoingspecifiedcourseslistedbytheconcernedBoSalongwithprerequisites. It is the responsibility of the student to acquire/completeprerequisitebefore taking the respective course.A student shall be permitted to choose only thosecoursesthathe/shehasnotstudiedinanyformduringtheProgramme.Theremaining4 credits must be acquired through two MOOCs courses. The courses must be ofminimum 8 weeks induration. Student has to acquire a certificate from the agenciesapproved by the BoS with grading or marks or pass. If the MOOC course is a passcourse without any grades, the grade to be assigned as decided by the AcademicCouncil.

xi)If a candidate drops (or terminated) from the Honors / Minor program, they cannotconvert the earned credits into free or core electives; they will remain extra. Theseadditional courses will find mention in the transcript (but not in the degreecertificate). Insuch cases, the student may choose between the actual grade or a "pass (P)" gradeand also choose to omit the mention of the course as for the following: All the coursessuccessfully completed under the dropped Minors will be shown in the transcript. Courses which were not completed under the droppedMinorwillnot beshowninthe transcript.

The credit contribution of these additional subjects to the computation of CGPA, however, would be considered as nil.

For offering Honors / Minor courses in any department as regular course work minimum 10 and 20 candidates are to be enrolled respectively. Else the courses are to be completed by MOOCS courses as suggested in the AICTE / APSCHE guidelines.

Track-1 VLSI

List of courses

S.No	Name of Course	Credits
1.	Analog IC Design	4
2.	Advanced VLSI Design	4
3.	Introduction to CAD for VLSI	4
4.	Low Power VLSI	4
5.	Design for Testability	4
6.	Hardware Security	4

Track-2 Embedded system Design

List of courses

S.No	Name of Course	Credits
1.	Advanced Embedded systems	4
2.	RTOs	4
3.	Advanced Microcontrollers	4
4.	IoT	4

Track-3 Advanced Communication Systems

List of courses

S.No	Name of Course	Credits
1.	EMI/EMC	4
2.	RF System Design	4
3.	Wireless broad band communications	4
4.	Multi carrier communication	4
5.	mm wave technology	4

Track-1 VLSI

List of courses

S.No	Name of Course	Credits
1.	Analog IC Design	4
2.	Advanced VLSI Design	4
3.	Introduction to CAD for VLSI	4
4.	Low Power VLSI	4
5.	Design for Testability	4
6.	Hardware Security	4

ANALOG IC DESIGN

ECE XXX **Credits:4**

Instruction: 3 periods & 1 Tutorial/Week Sessional Marks:40

End Exam: 3 Hours End Exam Marks:60

Prerequisites: Network Analysis and Synthesis, Electronic Circuits Analysis-I, Electronic Circuits Analysis-II

Course Outcomes:

At the end of the course, students will be able to

1.	Illustrate the basic MOS device physics and models
2.	Analyze and design single stage amplifiers
3.	Analyze and design differential amplifiers
4.	Analyze and design current sources/sinks/mirrors
5.	Analyze and design basic operational amplifiers circuits

SYLLABUS

UNIT-I **[12 Periods]**

BASIC MOS DEVICE PHYSICS

MOSFET as a switch, MOSFET structure and symbols, Threshold voltage, Derivation of I-V characteristics, second order effects.

UNIT-II **[12 Periods]**

DEVICE MODELING

DC Models, Small signal models, use of device models in circuit analysis, DC MOSFET model, and small signal MOSFET model, High frequency MOSFET Model, Measurement of MOSFET Model parameters.

UN IT-III **[12 Periods]**

SINGLE STAGE AMPLIFIERS

Basic concepts, CS stage with resistive load, CS stage with diode connected load, CS stage with Current-Source load, CS stage with Triode load, CS stage with Source degeneration, Source follower, Common gate stage, Cascode stage

UNIT-IV **[12 Periods]**

DIFFERENTIAL AMPLIFIERS

Single ended and differential operation, qualitative and quantitative analysis of Basic differential pair, common mode response, differential pair with MOS Loads

Passive and Active current mirrors: Basic current mirrors, Cascode current mirrors, Active current mirrors.

UNIT-V **[12 Periods]**

OPERATIONAL AMPLIFIERS

Performance parameters, one stage op-amps, two stage op-amps, gain boosting, common mode feedback, input range limitations, slew rate, power supply rejection.

TEXT BOOKS

1. Behzad Razavi, Design of Analog CMOS Integrated Circuits, Tata McGraw-Hill, 1st edition, 2002.

2. Randall Geiger, Phillip Allen, Noel Strader, VLSI Design Techniques for Analog and Digital Circuits, Tata McGraw-Hill, 1st edition, 2010.

REFERENCE BOOKS

1. Douglas R. Holberg, P. E. Allen Phillip E. Allen, CMOS Analog Circuit Design, 2nd edition, 2002

ADVANCED VLSI DESIGN

ECE XXX **Credits:4**

Instruction: 3 periods & 1 Tutorial/Week Sessional Marks:40

End Exam: 3 Hours End Exam Marks:60

Prerequisites: Basic VLSI fundamentals, Logic families

Course Outcomes:

At the end of the course, students will be able to

1.	Familiarization of CMOS logic families and layout rules
2.	Illustrate the advances beyond CMOS and super buffers
3.	Illustrate the small signal operation of MOSFETs and MESFETs
4.	Design various circuit layouts using NAND-NAND, NOR-NOR, AOI logic and their Technology mapping
5.	Illustrate the various CMOS design methodologies.

SYLLABUS

UNIT I **[9 Periods]**

OVERVIEW OF MOS CIRCUITS

MOS and CMOS static plots, CMOS logic families: static, dynamic and dual rail logic circuits; Integrated Circuit Layout: Introduction to CMOS Layout, Design Rules, Parasitic component in layout, latch-up, ESD Protection.

UNIT II **[9 Periods]**

BEYOND CMOS

Advances beyond CMOS, carbon Nano tubes, conventional vs. tactile computing, molecular and biological computing and diode- diode logic, Defect tolerant computing; Super Buffers-NMOS super buffer, tri state super buffer, CMOS super buffers.

UNIT III **[9 Periods]**

MIS STRUCTURES AND MOSFETS

MESFETS: MESFET and MODFET operations, quantitative description of MESFETS, small signal operation of MESFETS and MOSFETS; MIS systems in equilibrium, under bias.

UNIT IV **[9 Periods]**

SPECIAL CIRCUIT LAYOUTS AND TECHNOLOGY MAPPING

Introduction, Talley circuits, NAND-NAND, NORNOR, and AOI Logic, NMOS, CMOS Multiplexers, Barrel shifter, Wire routing and module lay out.

UNIT V **[9 Periods]**

SYSTEM DESIGN

CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, programmable logic, Programmable inter connect, programmable structure, Gate arrays standard cell approach, Full custom Design

TEXT BOOKS:

1. Kevin F Brennan “Introduction to Semi-Conductor Device”, Cambridge publications
2. Eugene D Fabricius “Introduction to VLSI Design”, McGraw-Hill publications.

REFERENCE BOOKS:

1. D.A Pucknell “Basic VLSI Design”, PHI Publication
2. Wayne Wolf, “Modern VLSI Design” Pearson Education, Second Edition
3. Addison Wesley N. Weste and K. Eshranghian, Principles of CMOS VLSI Design, 1985
4. L. Glaser and D. Dobberpuhl, Addison Wesley, The Design and Analysis of VLSI Circuits, ,1985

INTRODUCTION TO CAD FOR VLSI

ECE XXX **Credits:4**

Instruction: 3 periods & 1 Tutorial/Week Sessional Marks:40

End Exam: 3 Hours End Exam Marks:60

Prerequisites: Digital Electronics, VLSI design

Course Outcomes:

At the end of the course, students will be able to

1.	**Gain comprehensive** knowledge of VLSI design flow and automation
2.	**Familiarize** with the high-level synthesis process
3.	**Acquire** knowledge of logic synthesis process.
4.	**Explain** algorithms for floor planning, partitioning and placement
5.	**Explain** algorithms for routing.

SYLLABUS

UNIT-I **[9 Periods]**

INTRODUCTION TO DESIGN METHODOLOGIES

The VLSI Design Problem, The Design Domains, Design Actions, Design Methods and Technologies

Quick Tour of VLSI Design Automation Tools: Algorithmic and System Design, Structural and Logic Design, Transistor-level Design, Layout Design, Verification Methods, Design Management Tools

UNIT-II **[9 Periods]**

HIGH-LEVEL SYNTHESIS

Hardware Models for High-level Synthesis: Hardware for Computations, Data Storage, and Interconnection, Data, Control, and Clocks

Internal representation of the Input Algorithm: Simple Data Flow, Conditional Data Flow, Iterative Data Flow, Data-flow Graph Representation

Allocation, Assignment and Scheduling: Goals and Terminology, A detailed Example, Optimization Issues

Some Scheduling Algorithms: ASAP Scheduling, Mobility-based Scheduling, Force-directed Scheduling, List Scheduling

Some Aspects of the Assignment Problem: Optimization Issues, Graph Theoretical problem Formulation, Assignment by Interval and Circular-arc Graph Coloring, Assignment by Clique Partitioning

High-level Transformations

UNIT-III **[9 Periods]**

LOGIC SYNTHESIS AND VERIFICATION

Introduction to Combinational Logic Synthesis: Basic Issues and Terminology, A Practical Example

Binary-decision Diagrams: ROBDD Principles, ROBDD Implementation and Construction, ROBDD Manipulation, Variable Ordering, Applications to Verification, Applications to Combinatorial Optimization

Two-level Logic Synthesis: Problem Definition and Analysis, A Heuristic Based on ROBDDs

UNIT-IV **[9 Periods]**

FLOORPLANNING PLACEMENT AND PARTITIONING

Floor-planning Concepts: Terminology and Floorplan Representation, Optimization Problems in Floor-planning

Shape Functions and Floorplan Sizing

Placement and partitioning:

Circuit Representation, Wire Length Estimation Types of Placement Problem

Placement Algorithms: Constructive Placement, Iterative Improvement

Partitioning: The Kernighan-Lin Partitioning Algorithm.

UNIT-V **[9 Periods]**

ROUTING

Types of Local Routing Problems, Area Routing

Channel Routing: Channel Routing Models , The Vertical Constraint Graph , Horizontal Contraints and the Left-edge Algorithm, Channel Routing Algorithms

Introduction to Global Routing: Standard-cell layout, Building-block Layout and Channel Ordering

Algorithms for Global Routing : Problem Definition and Discussion, Efficient Rectilinear Steiner-tree Construction, Local Transformations for Global Routing.

TEXT BOOKS

1. Sabih H. Gerez, Algorithms for VLSI Design Automation, JOHN WILEY & SONS,1998

REFERENCE BOOKS

1. N.A. Sherwani, “Algorithms for VLSI physical design automation”, Kluwer Academic Publishers, 1999.

LOW POWER VLSI DESIGN

ECE XXX **Credits:4**

Instruction : 3 periods & 1 Tutorial/Week Sessional Marks:40

End Exam : 3 Hours End Exam Marks:60

Prerequisites: Digital Electronics, VLSI design

Course Outcomes:

At the end of the course, students will be able to

1.	Explain the sources of power dissipation in CMOS
2.	Classify the special techniques to mitigate the power consumption in VLSI circuits
3.	Summarize the power optimization and trade-off techniques in digital circuits.
4.	Illustrate the power estimation at logic and circuit level
5.	Explain the software design for low power in various level

SYLLABUS

UNIT-I **[9-Periods]**

POWER DISSIPATION IN CMOS

Sources of power dissipation – Physics of power dissipation in MOSFET devices: The MIS structure, long channel MOSFET, Submicron MOSFET , gate induced drain leakage– Power dissipation in CMOS : short circuit dissipation, dynamic dissipation, load capacitance– Low power VLSI design: Limits – principles of low power design, hierarchy of limits, fundamental limit, material limit, device limit, system limit.

UNIT-II **[9-Periods]**

POWER OPTIMIZATION USING SPECIAL TECHNIQUES

Power Reduction in Clock Networks: Clock Gating, Reduced Swing Clock, Oscillator Circuit for Clock Generation, Frequency Division and Multiplication, Other Clock Power Reduction Techniques - CMOS Floating Node: Tristate Keeper Circuit, Blocking Gate, Low Power Bus: Low Swing Bus, Charge Recycling Bus, Delay Balancing - Low Power Techniques for SRAM: SRAM Cell, Memory Bank Partitioning, Pulsed Word line and Reduced bit line Swing

UNIT-III **[9-Periods]**

DESIGN OF LOW POWER CIRCUITS

Transistor and Gate Sizing : Sizing an Inverter Chain, Transistor and Gate Sizing for Dynamic Power Reduction, Transistor Sizing for Leakage Power Reduction - Network Restructuring and Reorganization : Transistor Network Restructuring, Transistor Network Partitioning and Reorganization - Special Latches and Flip-flops : Self-gating Flip-flop, Combinational Flip-flop, Double Edge Triggered Flip-flop - Low Power Digital Cell Library : Cell Sizes and Spacing, Varieties of Boolean Functions, Adjustable Device Threshold Voltage

UNIT-IV **[9-Periods]**

POWER ESTIMATION

Modelling of signals - signal probability calculation - Statistical techniques - estimation of glitching power- Sensitivity analysis-Power estimation using input vector compaction, power dissipation in Domino logic, circuit reliability, power estimation at the circuit level, Estimation of maximum power: test generation based approach, steepest descent, generic based algorithm based approach

UNIT-V **[9-Periods]**

SOFTWARE DESIGN FOR LOW POWER

Sources of software power dissipation - software power estimation: Gate level, architecture level, bus switching activity, instruction level power analysis - software power optimization: minimizing memory access costs, instruction selection and ordering, power management - Automated low power code generation – Co-design for low power.

TEXT BOOKS:

1. Kaushik Roy and S.C.Prasad, "Low power CMOS VLSI circuit design", Wiley, 2000
2. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer,1995
3. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998

Reference Books:

1. DimitriosSoudris, Christians Pignet, Costas Goutis, "Designing CMOS Circuits for Low Power", Kluwer, 2002
2. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley 1999
3. AbdelatifBelaouar, Mohamed.I.Elmasry, "Low power digital VLSI design", Kluwer, 1995
4. James B.Kulo, Shih-Chia Lin, "Low voltage SOI CMOS VLSI devices and Circuits", John Wiley and sons, inc. 2001
5. Steven M.Rubin, "Computer Aids for VLSI Design", Addison Wesley Publishing

DESIGN FOR TESTABILITY

ECE XXX **Credits:4**

Instruction : 3 periods & 1 Tutorial/Week Sessional Marks:40

End Exam : 3 Hours End Exam Marks:60

Prerequisites: Nil

Course Outcomes:

At the end of the course, students will be able to

1.	Explain The Relationship Between Physical Failures and Fault Models and Model different types of faults in the digital circuits using appropriate fault models
2.	Use Efficient Logic And Fault Simulators for design verification and test evaluation
3.	Generate Test Patterns For Combinational Circuits Using Various Techniques
4.	Generate Test Patterns For Sequential Circuits Using Various Techniques
5.	Illustrate the various Design for Testability Methods.

SYLLABUS

UNIT I **[9 Periods]**

FAULT MODELING

Introduction, VLSI testing process and test equipment, Fault modeling: Defects, Errors, and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault-Fault Equivalence , Equivalence of Single Stuck-at Faults, Fault Collapsing, Fault Dominance and Checkpoint Theorem.

UNIT II **[9 Periods]**

LOGIC AND FAULT SIMULATION

Simulation for Design Verification , Simulation for Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-Value Simulation-Compiled-Code Simulation, Event-Driven Simulation .Algorithms for Fault Simulation ,Serial Fault Simulation, Parallel Fault Simulation , Deductive Fault Simulation , Concurrent Fault Simulation , Fault simulation for combinational circuits, Fault Sampling.

UNIT III **[9 Periods]**

COMBINATION CIRCUIT TEST GENERATION

Algorithms and Representations : Structural vs. Functional Test, Definition of Automatic Test-Pattern Generator, Search Space Abstractions, Algorithm Completeness, ATPG Algebras, Significant Combinational ATPG Algorithms -D-Calculus and D-Algorithm (Roth) , PODEM (Goel) ,Test Generation Systems, Test Compaction .

UNIT IV **[9 Periods]**

SEQUENTIAL CIRCUIT TEST GENERATION

ATPG for Single-Clock Synchronous Circuits: A Simplified Problem, Time-Frame Expansion Method, Simulation-Based Sequential Circuit ATPG, CONTEST Algorithm, Genetic Algorithms

UNIT V **[9 Periods]**

DESIGN FOR TESTABILITY

Controllability and observability, scan design, partial scan design, variations of scan. BUILT IN SELF TEST: BIST concepts, Test pattern generation for BIST exhaustive testing, Pseudorandom testing, pseudo exhaustive testing, constant weight patterns, Generic offline BIST Architecture, Boundary scan standard.

TEXT BOOKS:

1. Michael L. Bushnell, Vishwani D. Agrawal," Essentials of Electronic testing", Bell Labs, Lucent Technologies.
2. M. Abramovili, M.A. Breues, A. D. Friedman, "Digital Systems Testing and Testable Design", Jaico publications.
3. Fault Tolerant & Fault Testable Hardware Design-Parag K. Lala (PHI)

REFERENCE BOOKS:

1. Fault tolerant systems- Israel Koren, C.Manikrishna, Morgan Kaufmann, 2007.

HARDWARE SECURITY

ECE XXX **Credits:4**

Instruction : 3 periods & 1 Tutorial/Week Sessional Marks:40

End Exam : 3 Hours End Exam Marks:60

Prerequisites: DICD using HDLs, VLSI

Course Outcomes:

At the end of the course, students will be able to

1.	Analyze how digital system is specified, implemented, and optimized
2.	Explain VLSI testing
3.	Illustrate the hardware security and trust
4.	Detect and prevent hardware Trojans
5.	Counterfeit the ICs.

SYLLABUS

UNIT I **[9 Periods]**

DIGITAL SYSTEM DESIGN: BASICS AND VULNERABILITIES

Introduction, Digital System Specification, Digital System Implementation, Function Simplification and Don't Care Conditions, Sequential System Specification, Sequential System Implementation, Vulnerabilities in Digital Logic Design

UNIT II **[9 Periods]**

BACK GROUND ON VLSI TESTING

Introduction , test cost and product quality , test generation, structural DFT techniques: Design for testability, Scan design, Partial scan design, Boundary scan, BIST methods, ,At-speed delay Test.

UNIT III **[9 Periods]**

HARDWARE SECURITY AND TRUST

Hardware Trojans: Implementation, Taxonomy, Detection methodologies, activation methodologies. Counterfeit ICs. Hardware Trojan Attack, Taxonomy.

UNIT IV **[9 Periods]**

HARD WARE TROJAN DETECTION AND PREVENTION

A Case Study for Hardware Trojan Detection in Third-Party Digital IP Cores ,Detection and Prevention at Register Transfer level, gate level

UNIT V **[9 Periods]**

COUNTERFEIT ICS

Taxonomy, Assessment, challenges, Path delay finger printing :degradation analysis, degradation analysis, finger print considering aging. Statistical data analysis, Process and temperature variation analysis.

TEXT BOOKS:

1. Mohammad Tehranipoor-Cliff wang editors, Introduction to hardware security and trust , Springer Science & Business Media ,sep 2011
2. Mohammed Tehranipoor,Hassan salmani,Xuehui Zhang, Integrated Circuit Authentication ,Hardware Trojans and Counterfeit Detection, Springer International Publishing Switzerland 2014

REFERENCE BOOKS:

1. Hassan Salmani, Trusted Digital Circuits Hardware Trojan Vulnerabilities, Prevention and detection Springer International Publishing AG, part of Springer Nature 2018

Track-2 Embedded system Design

List of courses

S.No	Name of Course	Credits
1.	Advanced Embedded systems	4
2.	RTOs	4
3.	Advanced Microcontrollers	4
4.	IoT	4

ADVANCED EMBEDDED SYSTEMS

ECE XXX **Credits:4**

Instruction : 3 periods & 1 Tutorial/Week Sessional Marks:40

End Exam : 3 Hours End Exam Marks:60

Prerequisites: Microprocessors & Microcontrollers

Course Outcomes:

At the end of the course, students will be able to

6.	Analyze and Evaluate the Embedded system design flow from the requirements to the deployment level and analyze the hardware/software tradeoffs involved in the design of embedded systems.
7.	Acquire knowledge of the architecture of ARM 32-bit microcontroller
8.	Acquire knowledge of the instruction set of ARM 32-bit microcontroller
9.	Program ARM 32-bit microcontroller to meet the requirements of the user
10.	Analyze various applications

SYLLABUS

UNIT-I **[10 Periods]**

EMBEDDED COMPUTING

Introduction, Complex Systems and Microprocessors, The Embedded System Design Process, Formalisms for System Design

UNIT-II **[12 Periods]**

ARM-32 BIT MICROCONTROLLER

Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence

UN IT-III **[12 Periods]**

INSTRUCTION SETS

Assembly basics, Instruction list and description, useful instructions, Memory Systems, Memory maps, Cortex M3 implementation overview, pipeline and bus interface

UNIT-IV **[10 Periods]**

CORTEX-M3 PROGRAMMING

Exceptions, Nested Vector interrupt controller design, Systick Timer, Cortex-M3 Programming using assembly and C language, CMSIS

UNIT-V **[9 Periods]**

CASE STUDIES/INDUSTRIAL APPLICATIONS

Model Train Controller - Data Compressor - Alarm Clock: Requirements, Specification, Design and Testing

TEXT BOOKS

1. Wayne Wolf, Computers as Components-principles of Embedded computer system design, 2nd Edition, Elsevier
2. Joseph Yiu, The Definitive Guide to the ARM Cortex-M, 2nd edn, Newnes-Elsevier, 2010.

REFERENCE BOOKS

1. David E. Simon, An Embedded Software Primer, Pearson Education
2. Frank Vahid, Tony Givargis, Embedded System Design, 2nd Edition, John Wiley.

REAL TIME OPERATING SYSTEMS

ECE XXX **Credits:4**

Instruction : 3 periods & 1 Tutorial/Week Sessional Marks:40

End Exam : 3 Hours End Exam Marks:60

Prerequisites: Microcontrollers, C Programming, FIFO queues, and Operating Systems

Course Outcomes:

At the end of the course, students will be able to

6.	Analyse theoretical and practical concepts, and functioning of real time operating system
7.	Distinguish a real-time operating system from other systems
8.	Explain the specifications, design requirements and kernel techniques in development of RTOS
9.	Evaluate the real time operating systems based on real time applications
10.	Implement the real-time operating system principles.

SYLLABUS

UNIT I **[12 Periods]**

INTRODUCTION TO RTOS

Introduction and classification of Real Time Operating System, Types of Real Time Operating Systems, Human Computer Interaction in Real Time Systems, BIOS and Boot Process, real-time design issues, examples, Hardware Considerations: logic states, CPU, memory, I/O, Architectures, RTOS building blocks

UNIT II **[12 Periods]**

REAL -TIME KERNELS

Introduction, Polled loop with interrupts, Coroutines, Interrupt Driven systems, context switching, Round-Robin system, preemptive priority systems, Major and minor cycles, hybrid systems, foreground /background systems, Real time operation, Full-Featured real- Time operating systems, Task control block model, task management, posix.

UNIT III **[10 Periods]**

PROCESS MANAGEMENT OF RTOS

Concepts, scheduling, IPC, RPC, CPU Scheduling, scheduling criteria, scheduling algorithms, Threads: Multi-threading models, threading issues, thread libraries, synchronization Mutex: creating, deleting, prioritizing mutex, mutex internals

UNIT-IV **[12 Periods]**

PROCESS SYNCHRONIZATION OF RTOS

Messages, Buffers, mailboxes, queues, semaphores, deadlock, priority inversion

Memory Management of RTOS:

Process stack management, run-time buffer size, swapping, overlays, block/page management, replacement algorithms, real-time garbage collection

UNIT V **[7 Periods]**

Fault – Tolerant Design: A Case Study, Case Study in Software Requirements Specification for Four way, Traffic Intersection Traffic Light Controller System.

TEXT BOOKS:

1. Real-Time Systems Design and Analysis–3rd Edition, Phillip A. Laplante. Apr 2004.

2. Embedded systems architecture, Programming and design-3rdEdition,Raj Kamal. 2017
3. J. J Labrosse, “MicroC/OS-II: The Real –Time Kernel”, Newnes, 2002.
4. Jane W. S. Liu, “Real-time systems”, Prentice Hall, 2000.

REFERENCE BOOKS:

1. Real Time Systems- C.M. Krishna, Kang G.Shin McGraw-Hill, 1997.
2. Embedded Real Time system-Concepts, Design and Programming, Dr. K. V. K. K. Prasad, Dream Tech Pres, New Delhi 2003.
3. Doug Abbott, “Linux for Embedded and Real-Time Applications”, Newnes, 2nd Edition, 2011.

ADVANCED MICROCONTROLLER

ECE XXX **Credits:4**

Instruction : 3 periods & 1 Tutorial/Week Sessional Marks:40

End Exam : 3 Hours End Exam Marks:60

Prerequisites: Microprocessors and Microcontrollers

Course Outcomes:

At the end of the course, students will be able to

6.	Familiarize the features, specification of modern microprocessors
7.	Acquire salient features of CISC microprocessors based on IA-32 bit and IA-64 bit architectures
8.	Acquire salient features of RISC processors based on ARM architecture and different application profiles of ARM core
9.	Acquire knowledge about ARM – M3 architecture and its salient features
10.	Acquire knowledge about MSP-EXP430F5529LP architecture and its salient features

SYLLABUS

UNIT-I **[9 Periods]**

ADVANCED FEATURES OF MICROPROCESSORS

Evolution of microprocessors - Data and Address buses – clock speed – memory interface - multi-core architectures – cache memory hierarchy – operating modes – super scaler execution – dynamic execution – over-clocking – integrated graphics processing - performance benchmarks.

UNIT-II **[9 Periods]**

HIGH PERFORMANCE CISC ARCHITECTURES

Introduction to IA-32 architecture – Intel Pentium Processors family tree – Memory Management – Branch prediction logic - Superscalar architecture – Hyper threading technology – 64 bit extension technology – Intel 64 bit architecture - Intel Core processor family tree – Turbo boost technology – Smart cache - features of Nehalem microarchitecture

UNIT-III **[9 Periods]**

HIGH PERFORMANCE RISC ARCHITECTURE – ARM

RISC architecture merits and demerits – The programmer's model of ARM Architecture – 3- 89 stage pipeline ARM organization - 3-stage pipeline ARM organization – ARM instruction execution – Salient features of ARM instruction set - ARM architecture profiles (A, R and M profiles).

UNIT-IV **[9 Periods]**

ARM CORTEX PROCESSORS

Introduction to the Cortex-M Processor Family - ARM 'Cortex-M3' architecture for microcontrollers – Thumb 2 instruction technology – Internal Registers - Nested Vectored Interrupt controller - Memory map - Interrupts and exception handling – Applications of CortexM3 architecture.

UNIT-V **[9 Periods]**

MSP430 MICROCONTROLLERS

Functional Block diagram of MSP-EXP430F5529LP - Memory Mapped CPU, Exceptions, Architecture of MSP430 - Processor Addressing Modes - Instruction Set, Interrupts, Digital in-outs, Timer, Communication interfaces.

TEXT BOOKS

1. Barry B Breg, The Intel Microprocessors, PHI, 2008.
2. Steve Furber, ARM System – On – Chip architecture, Addision Wesley, 2000.

REFERENCE BOOKS

1. Intel Inc, Intel 64 and IA-32 Architectures Developers Manual, Volume-I, 2016.
2. Joseph Yiu, The Definitive Guide to the ARM ® Cortex-M3, Newnes, 2010.
3. John H Davies, MSP430 Microcontroller Basics, Elsevier, 2008.
4. Trevor Martin, The Designers Guide to the Cortex-M Processor Family, Newnes,2013.
5. Manuel Jimenez, Rogelio Palomera and Isidoro Convertier, Introduction to Embedded systems using Microcontrollers and the MSP430, Springer 2014.

INTERNET OF THINGS (IoT)

ECE XXX **Credits:4**

Instruction : 3 periods & 1 Tutorial/Week Sessional Marks:40

End Exam : 3 Hours End Exam Marks:60

Prerequisites: Nil

Course Outcomes:

At the end of the course, students will be able to

6.	Describe internet of Things and its hardware and software components
7.	Interpret Design Principles for connected devices
8.	Interface I/O devices, sensors & communication modules
9.	Remotely monitor data and control devices
10.	Develop real life IoT based projects

SYLLABUS

UNIT I **[10 Periods]**

Overview of Internet of Things:

Internet of Things, IoT Conceptual Framework, IoT Architectural view, Technology Behind IoT, Source of IoT, M2M communication, Examples of IoT

UNIT II **[10 Periods]**

Design Principles for connected devices

Introduction, IoT/M2M systems layers and Design standardization, Communication technologies, Data enhancement, Data consolidation and Device management at Gateway, Ease of designing and affordability.

UNIT III **[10 Periods]**

Sensors, Participatory Sensing, RFIDs and Wireless Sensor Networks

Introduction, Sensor technology, Participatory Sensing, Industrial IoT and Automotive IoT, Actuators, Sensor Data Communication Protocols, RFID technology, WSN Technology.

UNIT IV **[10 Periods]**

Prototyping the Embedded Devices for IoT and M2M

Introduction, Embedded Computing basics, Embedded Platforms for prototyping, Things always connected to the Internet/Cloud.

UNIT-V **[10 periods]**

IoT case studies and mini projects based on Industrial automation, Transportation, Agriculture, Healthcare, Home Automation

TEXT BOOKS:

1. Raj Kamal, “Internet of Things: Architecture and Design”, McGraw Hill
2. Cuno Pfister, “Getting Started with the Internet of Things”, O Reilly Media

REFERENCE BOOKS:

1. Vijay Madisetti, Arshdeep Bahga, Ïnternet of Things, “A Hands on Approach”, University Press.

2. Hakima Chaouchi, “ The Internet of Things Connecting Objects to the Web” ISBN : 978-1-84821-140-7, Willy Publications.

Track-3 Advanced Communication Systems

List of courses

S.No	Name of Course	Credits
1.	EMI/EMC	4
2.	RF System Design	4
3.	Wireless broad band communications	4
4.	Multi carrier communication	4
5.	mm wave technology	4

ELECTROMAGNETIC INTERFERENCE / COMPATABILITY

ECE XXX **Credits:4**

Instruction : 3 periods & 1 Tutorial/Week Sessional Marks:40

End Exam : 3 Hours End Exam Marks:60

Prerequisites: Nil

Course Outcomes:

At the end of the course, students will be able to

11.	Apply the knowledge of HDL for modeling and functional verification of Digital circuits.
12.	Analyze digital circuits using gate level and data flow Verilog HDL modeling
13.	Analyze digital circuits using behavioral Verilog HDL modeling
14.	Design and synthesize a digital circuit for complex systems using Verilog HDL
15.	Program and synthesize a given problem statement using state machines and Verilog HDL

SYLLABUS

UNIT I **[9 Periods]**

INTRODUCTION EMI/EMC/ESD/EMP: EM environment, Historical Notes, Problems of EMI, Frequency Conservation, Assignment & spectrum, practical experiences, Occurrence of EMI, Concepts of EMI/EMC-definitions, Sources of noise, Natural and Nuclear Sources of EMI, Conducted and Radiated Emissions and Susceptibility. EMI Testing and Compliance Tests, ESD, EMP- Introduction.

UNIT II **[9 Periods]**

CONDUCTED EMI/EMC: Origin of Conducted EMI, Common and Normal mode Noise, Noise from Power Electronic Systems, Spectra of Pulse Noise Sources, Modeling of EMI Noise Sources, Transient Disturbance Simulation Signals, EMI Filters for Mains Noise.

EMC Regulation/ Standards- I : FCC, CISPR/IEC, VDE

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UNIT III **[9 Periods]**

RADIATED EMI/EMC: Introduction, Open Air Test Site (OATS) measurements, measurement precautions open air test site, terrain roughness, normalized site attenuation measurement of test site imperfections, Antenna factor measurement, measurement errors

EMC Regulation/ Standards-II- IEEE/ ANSI, MIL-STD

UNIT-IV **[9 Periods]**

ELIMINATION/REDUCTION METHODOLOGIES: Grounding Techniques, Shielding Techniques, Electrical Bonding Techniques, Cabling Techniques, Connectors and Components/ Accessories.

UNIT V **[9 Periods]**

EMI/EMC MEASUREMENT TECHNOLOGIES:

Introduction to various instruments used in the measurements and their characteristics, Radiated Interference Measurements, Conducted Interference Measurements, Pitfalls in EMI Measurements, Measurements of pulsed EMI, Introduction of Measurement Environment –

OATS, Anechoic Chamber, TEM, GTEM cell. Software in EMI/EMC Measurements, Different EMI Test Instruments and their comparisons.

TEXT BOOKS:

1. J Kodali, V.P., "Engineering EMC- Principles, Measurements, Technologies and Computer Models", 2nd Ed., IEEE Press, NY, 2000.
2. IMPACT, EMI/EMC for Engineering Colleges, RSTE ,1997.

REFERENCE BOOKS:

1. Paul, R.C, "Introduction to EMC", 2nd Ed., John Wiley & Sons Inc., 2006.

RF SYSTEM DESIGN

ECE XXX **Credits:4**

Instruction : 3 periods & 1 Tutorial/Week Sessional Marks:40

End Exam : 3 Hours End Exam Marks:60

Prerequisites: Nil

Course Outcomes:

At the end of the course, students will be able to

11.	Understand the Radio frequency design concept and impart knowledge on various types of communication system architecture.
12.	Analyze various parameters of RF circuits with in a communication system.
13.	Develop an insight to make use of several high frequency RF design techniques.
14.	Utilize the various RF circuit design concepts in designing the RF Amplifier.
15.	Utilize the various RF circuit design concepts in designing the RF Oscillator.

SYLLABUS

UNIT I **[9 Periods]**

RF AND MICROWAVE CONCEPTS AND APPLICATIONS: Introduction, Reasons for using RF/Microwaves, RF/Microwave applications, Radio frequency waves, RF and Microwave circuit design, The unchanging fundamentals versus the ever-evolving structure, General active circuit block diagrams.

UNIT II **[9 Periods]**

RF ELECTRONICS CONCEPTS: Introduction, RF/Microwaves versus DC or low AC signals, EM spectrum, Wave length and frequency, Circuit representation of two port RF/microwave networks. Basics of RF component, Resonant circuits, Analysis of a simple circuit in phasor domain, Impedance transformers, RF impedance matching, Three element matching.

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UNIT III **[9 Periods]**

SMITH CHART AND ITS APPLICATIONS: Introduction, A valuable graphical aid the smith chart, Derivation of smith chart, Description of two types of smith charts, Smith charts circular scales, Smith charts radial scales, The normalized impedance-admittance (ZY) smith chart introduction, Applications of the smith chart - Distributed circuit applications, Lumped element circuit applications.

UNIT-IV **[9 Periods]**

RF AND MICROWAVE AMPLIFIERS SMALL AND LARGE SIGNAL DESIGN: Introduction, Types of amplifiers, Small signal amplifiers, Design of different types of amplifiers, Multistage small signal amplifier design.

Introduction, High-power amplifiers, Large signal amplifier design, Microwave power combining/dividing techniques, Signal distortion due to inter modulation products, Multistage amplifiers, Large signal design

UNIT V **[9 Periods]**

RF AND MICROWAVE OSCILLATOR DESIGN: Introduction, Oscillator versus amplifier design, Oscillation conditions, Design of transistor oscillators, Generator-tuning networks.

TEXT BOOKS:

1. Mathew M. Radmanesh , "Radio Frequency and Microwave Electronics", Person Education Inc., New Delhi
2. Pozar, D.M., "Microwave and RF Design of Wireless Systems", John Wiley & Sons, 2001.

REFERENCE BOOKS:

1. Joseph Helszain, "Microwave Engineering, Active and Non-reciprocal Circuits", McGraw Hill International Edition, 1992

WIRELESS BROADBAND COMMUNICATIONS

ECE XXX **Credits:4**

Instruction : 3 periods & 1 Tutorial/Week Sessional Marks:40

End Exam : 3 Hours End Exam Marks:60

Prerequisites: Computer Network Engineering

Course Outcomes:

At the end of the course, students will be able to

11.	Explain the Fundamental Concepts & Components of Broadband Communication
12.	Analyze various Basic Broadband Network Architectures
13.	Analyze various Advanced Broadband Network Architectures
14.	Get exposed to the changes in Wireless Data Services with respect to Generations
15.	develop a brief theoretical foundation on Personal Communications Systems & their services making use of Mobile Satellites

SYLLABUS

UNIT-I **[9 Periods]**

Fundamental Concepts of Broadband Communication:

Components of Broadband Communication Systems, Communications Network Architecture, Cable Broadband Data Network Architecture, The Importance of Broadband Network Architectures, The Future of Broadband Telecommunications, Internetworking Standards.

UNIT-II **[9 Periods]**

Network Architectures-I:

General Network Architectures of INTERNET, INTRANET, EXTRANET, FIBER CHANNEL, SYNCHRONOUS OPTICAL NETWORK (SONET), VIRTUAL PRIVATE NETWORK (VPN).

UNIT-III **[9 Periods]**

Network Architectures-II:

ISDN, ASYNCHRONOUS TRANSFER MODE (ATM), DIGITAL SUBSCRIBER LINE SYSTEMS, Interactive Set-Top Cable Box & Accessing Internet through CABLE MODEM SYSTEM, Comparison between Broadband DSL and Cable Modem Technologies.

UNIT-IV **[9 Periods]**

WIRELESS DATA SERVICES:

Wireless LAN, Wireless ATM, Wireless PAN, Cellular Communications, Cellular Digital Packet Data, WiMAX, Wireless Standards, Generations of Wireless Networks.

UNIT-V **[9 Periods]**

PERSONAL COMMUNICATIONS SERVICE:

Personal Communications Systems, Basic Features of PCS, PCS Solutions, PCS Architecture, PCS Standard, PCS Satellite Services, PCS Access Methods, Broadband Airborne Mobile Satellite Communication.

TEXT BOOKS

1. "Introduction to Broadband Communication Systems" by Cajetan M. Akujuobi, Matthew N.O. Sadiku, 1st Edition, Published by Chapman and Hall/CRC, 2007.
2. "Broadband Communications" by Robert Newman, Prentice Hall, 2002.

REFERENCE BOOKS

1. Jochen H.Schiller, "Mobile Communications", 2nd Edition, Pearson, 2014.

MULTI CARRIER COMMUNICATION SYSTEMS

ECE XXX **Credits:4**

Instruction : 3 periods & 1 Tutorial/Week Sessional Marks:40

End Exam : 3 Hours End Exam Marks:60

Prerequisites: Cellular Mobile Communication

Course Outcomes:

At the end of the course, students will be able to

11.	Identify the problems faced in SISO and apply solutions to overcome different issues faced in SISO through MIMO.
12.	Analyze the spatial multiplexing properties of MIMO.
13.	Design and construct Real & Complex orthogonal and Quasi orthogonal STBC
14.	Apply the fundamental concepts of Multicarrier Communication to design an LTE Systems.
15.	Identify the Challenges in Multicarrier Systems like PAPR & Analyze various reduction Techniques.

SYLLABUS

UNIT-I: **[9-Periods]**

Theoretical concepts of MIMO:

Review of SISO fading communication channels , Multiple Antennas and Space-Time Communications. MIMO channel models-Classical i.i.d models, Frequency selective and Extended channels, Capacity of MIMO channels-Ergodic and outage capacity.

UNIT-II: **[9-Periods]**

MIMO Diversity and Spatial Multiplexing:

Sources and types of diversity, analysis under Rayleigh fading, Diversity and channel knowledge. Alamouti space time code, MIMO spatial multiplexing. Space time receivers. ML, ZF, MMSE and Sphere decoding, BLAST receivers and Diversity multiplexing trade-off.

UNIT-III: **[9-Periods]**

Space Time Block Codes:

Code design criteria for quasi-static channels (Rank, determinant and Euclidean distance), Space time block codes on real and complex orthogonal designs: Orthogonal designs, Generalized orthogonal designs, Quasi-orthogonal designs and Performance analysis. Representation of STTC, Delay diversity as a special case of STTC and Performance analysis.

UNIT-IV: **[9-Periods]**

Communication with Multi carrier Modulation:

Data Transmission Using Multiple Carriers, Multicarrier Modulation with Overlapping Subchannels, Discrete Implementation of Multicarrier Modulation-OFDM system model - FFT implementation , Channel capacity and OFDM, Comparison with single carrier.

UNIT-V: **[9-Periods]**

Challenges in Multicarrier Communication:

Timing and Frequency Offset in OFDM-Pilot and Non pilot based methods. Challenges in Multicarrier Systems-PAPR properties of OFDM,PAPR-Reduction with Signal Distortion-

signals – PAPR reduction techniques with signal distortion; Techniques for distortion less PAPR reduction – Selective mapping and Optimization techniques.

Text Books:

1. David Tse and Pramod Viswanath, "Fundamentals of Wireless Communication", Cambridge University Press 2005.
2. E.G. Larsson and P. Stoica, "Space-Time Block Coding for Wireless Communications", Cambridge University Press 2008.
3. Y. Li. G. Stuber, "OFDM for Wireless Communication", Springer, 2006.

Reference Books:

1. Ezio Biglieri, Robert Calderbank et al "MIMO Wireless Communications" Cambridge University Press 2007.
2. Hamid Jafarkhani, "Space-Time Coding: Theory and Practice", Cambridge University Press 2005.

MILLIMETRE WAVE TECHNOLOGY

ECE XXX **Credits:4**

Instruction : 3 periods & 1 Tutorial/Week Sessional Marks:40

End Exam : 3 Hours End Exam Marks:60

Prerequisites: Microwave Theory & Techniques

Course Outcomes:

At the end of the course, students will be able to

6.	Able to explain the fundamental concepts of Mm Wave Wireless Communication.
7.	Able to analyze various channel effects in Mm Wave communication scenario and understand various design considerations.
8.	To get exposed to the goals and challenges of new emerging applications of Mm Wave in Wireless Communications.
9.	Able to analyze challenges and various emerging applications of Mm Waves in Wireless Communications research field
10.	Able to review the literature related to Mm wave for Wireless Communication and to report it ethically.

SYLLABUS

UNIT-I **[9 Periods]**

INTRODUCTION

A Preview of MmWave Implementation Challenges, material properties at millimetre wave frequencies, guiding structures, Emerging Applications of MmWave Communications, MmWave Standardization.

UNIT-II **[9 Periods]**

RADIO WAVE PROPAGATION FOR mmWAVE

Large-Scale Propagation Channel Effects, SmallScale Channel Effects, Spatial Characterization of Multipath and Beam Combining, Angle Spread and Multipath Angle of Arrival, Antenna Polarization, Outdoor and Indoor Channel Models.

UNIT-III **[9 Periods]**

ANTENNAS AND ARRAY FOR mmWAVE APPLICATIONS

Fundamentals of On-Chip and In-Package MmWave Antennas, Fundamentals of On-Chip and In-Package MmWave Antennas, InPackage Antennas, Antenna Topologies for MmWave Communications, Techniques to Improve Gain of On-Chip Antennas, Adaptive Antenna Arrays — Implementations for MmWave Communications, Characterization of On-Chip Antenna Performance.

UNIT-IV **[9 Periods]**

MULTI-GBPS DIGITAL BASEBAND CIRCUITS

Review of Sampling and Conversion for ADCs and DACs, Device Mismatches: An Inhibitor to ADCs and DACs, Goals and Challenges in ADC Design, Encoders, Trends and Architectures for MmWave Wireless ADCs, Digital to Analog Converters.

UNIT-V **[9 Periods]**

mmWAVE PHYSICAL LAYER DESIGN AND ALGORITHMS

Practical Transceivers, High-Throughput PHYs, PHYs for Low Complexity, High Efficiency, Future PHY Considerations, Challenges when Networking mmWave Devices.

TEXTBOOKS:

1. Theodore S. Rappaport, Robert W. Heath Jr., Robert C. Daniels, James N. Murdock, Millimeter Wave Wireless Communications, Prentice Hall, 2014.

REFERENCE BOOKS:

1. Prakash Bhartia, and Inder Bahl, MmWave Engineering and Applications, WileyInterscience